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(71)Applicant : SGS THOMSON MICROELECTRON SA

(72)Inventor : TAILLIET FRANCOIS

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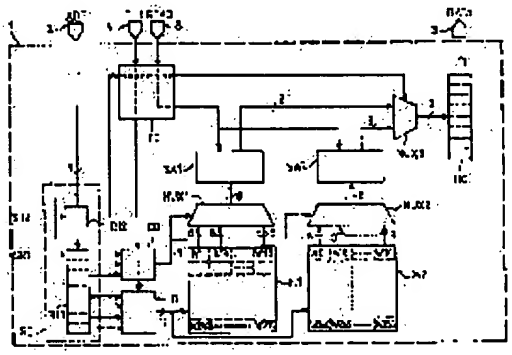
(54) METHOD AND MEMORY FOR PREDICTIVE READ OF SERIAL ACCESS MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To increase a maximum permissible internal access time and equalize an access time which is viewed from outside equal to that of standard constitution by making an address begin to be decoded according to the starting (q) bits of the address.



SOLUTION: The starting (q) bits of the address ADD are stored in a subregister RI1 and the remaining (p) bits are stored in R12. When a word is read out, (q) bits of the word are decoded by a row decoding circuit LD and a column decoding circuit CD while the (q) and (p) address bits of the word are stored in the RI's, and binary information represented with the respective words in half arrays M1 and M2 is fetched to sense circuits SA1 and SA2. A control circuit CC decodes the (p) bits and the binary information of their word is derived to a terminal 3 by a multiplexer MUXS and an output register RO.

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(71)出願人　591095720
エスジェーエスートムソン　ミクロエレクトロニクス　ソシエテ　アノニム
SGS-THOMSON MICROELECTRONICS SOCIETE ANONYME
フランス国　94250　ジャンティイ　アヴニュガリエニ　7

(72)発明者　フランソワ　テリエ
フランス国　93800　エピネイ　スュル　セーヌリュ　ガブリエル　ペリ　49

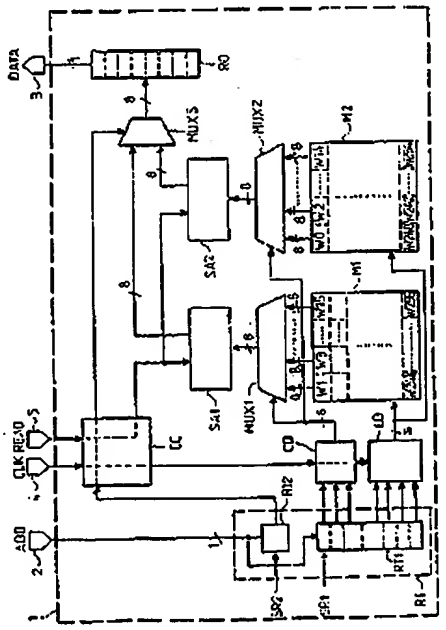
(74)代理人　弁理士　越場　隆

(54)【発明の名称】　シリアルアクセスメモリの予測読出し方法及びそのためのメモリ

(57)【要約】

【課題】　アドレスビットがまだすべて受けられていないとき、アドレス復号が開始されるような、メモリの読出し方法を開示する。

【解決手段】　部分的に復号されたアドレスに対応するすべての情報要素が取り出され、残りのアドレスビットが受けられると、完全なアドレスに対応する情報要素が選択される。従って、情報要素を取り出すための最大許容時間が、内部的に増大される。しかし、メモリの外部から見たこの時間は、所与の周波数に対して同じままである。この開示はまた、この方法を実行するメモリに関する。



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【特許請求の範囲】

【請求項１】　各メモリが複数ワードにマトリクスの形に構成されており、各ワードの内容が２進情報要素を表し、各ワードがｋビットに２進モードで符号化されたアドレスでアクセスでき（ｋは１より大きい整数）、アドレスビットがアドレス入力端子を介してメモリにシリアルに供給される、集積回路メモリのワードの内容を読出す方法であって、１ワードの内容を読出すために、

読出したい１ワードのアドレスの初めのｑビットをシリアルに受けて（ｑはｋより小さい整数）、

前記アドレスの残りの〔ｋ－ｑ〕ビットを受けることと並行して、前記受けたアドレスの前記初めのｑビットを復号し、前記受けたアドレスの前記初めのｑビットに対応する初めのｑアドレスビットを有するワードに読出し回路を接続し、前記ワードの内容が表す２進情報要素を取り出し、

読出したい１ワードの前記アドレスの前記残りの〔ｋ－ｑ〕ビットを復号すると共に、前記受けたアドレスの前記初めのｑビットに対応するアドレスビットを有する前記ワードの前記内容が表す前記２進情報要素を、メモリのデータ出力端子に出力することを特徴とする集積回路メモリのワードの内容を読出す方法。

【請求項２】　メモリは、第１のアドレスに対応する第１のワードの内容の読出し後、メモリの第２ワードの内容により表される第２の２進情報要素をデータ出力端子に自動的に出力するシーケンシャル読出しモードを有することを特徴とする請求項１記載の方法。

【請求項３】　第２のワードのアドレスの復号を、第１ワードの内容により表される２進情報をデータ出力端子に出力している間に、行うことを特徴とする請求項２記載の方法。

【請求項４】　シーケンシャル読出しモードで、一度に１つの２進情報要素を取り出すことを特徴とする請求項２から３のいずれかに記載の方法。

【請求項５】　複数ワードに構成されており、各ワードの内容が２進情報要素を表し、各ワードが、ｋビットに２進モードで符号化されたアドレスでアクセスできる（ｋは１より大きい整数）、集積回路メモリであって、

アドレスビットをシリアルに受けるアドレス入力端子と、

アドレスされたワードの内容に対応する２進情報要素を出力するデータ出力端子と、

受けたアドレスビットを記憶する入力レジスタと、

受けたアドレスビットを復号する回路と、

ワードを読出す回路に接続する回路とを具備している集積回路メモリにおいて、

前記ワードが、複数のワード群に構成されており、各ワード群に含まれるワードの初めのｋアドレスビットが互いに異なり、残りの〔ｋ－ｑ〕アドレスビットが同一であり（ｑはｋより小さい整数）、

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各ワード群ごとに読出し回路が設けられ、メモリがｋアドレスビットを受けると、受けた初めのｋアドレスビットに対応するワード群の内容により表される２進情報を前記読出し回路が取り出し、

メモリが更に、受けたｋビットに対応するアドレスを有するワードの内容により表される２進情報を、前記データ出力端子に出力する制御出力マルチプレクシング回路を具備していることを特徴とする集積回路メモリ。

【請求項６】　入力レジスタは、それぞれｑ個のセルと〔ｋ－ｑ〕個のセルから形成された２つのシフトサブレジスタにより構成されていることを特徴とする請求項５記載のメモリ。

【請求項７】　入力レジスタは、２進アドレスカウンタであることを特徴とする請求項６記載のメモリ。

【請求項８】　制御回路は、入力レジスタの内容を変更する手段を備えることを特徴とする請求項７記載のメモリ。

【請求項９】　読出し回路により取り出された２進情報要素を格納するために、読出し回路に接続された出力レジスタを備えることを特徴とする請求項５から８のいずれか１項に記載のメモリ。

【請求項１０】　電気的にプログラマブルで消去可能メモリであることを特徴とする請求項５から９のいずれか１項に記載のメモリ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はシリアルアクセスメモリに関する。特に、本発明は、他の形式の揮発性または非揮発性のメモリに適応できるが、電気的に消去可能なプログラマブル読出し専用メモリ（ＥＥＰＲＯＭｓ）に関する。

【０００２】

【従来の技術】（記憶される情報要素の数の見地から）きわめて大きい情報記憶容量を有する集積回路形式のメモリの現在の開発は、これら集積回路メモリを組み込んだシステムの動作速度を決定するクロック信号の周波数を高くしたい要望により進められている。その結果、同時に、これらメモリを構成するワードの内容にアクセスする時間をますます短くする研究もある。ここで"ワード"とは、ｂビットに符号化された２進情報要素を表す内容を持つ物理的実体を意味する。ここでｂは整数である。典型的には、ワードは、ｂ個の基本メモリセルにより形成され、各基本メモリセルは典型的には記憶回路により形成される。

【０００３】アクセス時間よりみて、パラレルアクセスメモリは最も有利なメモリである。このようなメモリの動作速度を決定するクロック信号の１サイクルに対応する周期は、内容が読出されるワードの１つのアドレスを、並行して、これらメモリの１つを与えるに十分である。

【０００４】それにもかかわらず、シリアルアクセスメモリはまた，製造価格が低いこと、とりわけパッケージが明らかに小さく軽いことなど、パラレルアクセスメモリと比較して明らかな利点がある。事実、シリアルメモリが必要な接続ピンの数はきわめて少ない。集積回路の接続ピン数は，集積回路が占めるスペース量にきわめて影響を与える。その結果，シリアルアクセスメモリは携帯用ではきわめて有用である。

【０００５】しかし、これらシリアルアクセスメモリのクロック信号周波数および記憶容量を増大できることが望ましい。現在最も高性能な製品は，記憶容量が６４キロビットで，１メガヘルツ程度の周波数で動作する。近い将来、約２５６キロビットの記憶容量と５メガヘルツ範囲以上の周波数が期待できる。

【０００６】実際には、これらメモリのクロック信号周波数の増大は，読出しモードでの、ワードの内容に対するアクセス時間に本質的に係わる技術的問題が生じる。"読出しモード"での"アクセス時間"とは、ワードのアドレスがメモリに知られた時点（すなわち、ワードのアドレスビットの全てをメモリがシリアルに受けた時点）と、ワードのメモリセルの内容が表す２進情報が（メモリがシリアル出力メモリである場合）利用可能になり始めた時点，または（メモリがパラレル出力メモリであるかまたは情報要素が１ビットに符号化されている場合）１つ以上の出力ピンを介してメモリの外部で利用可能となる時点との間の，外部で見た期間を意味すると理解されたい。

【０００７】アクセス時間は、次の２つの段階を順番に実行するのに必要な時間によって本質的に制限される。

・　メモリが受けたアドレスを復号すること、すなわち，読出したい２進情報を表す内容を有するワードに読出し回路を接続するための様々な切換え装置を適切に切り換えること。

・　本来の読出しプロセス，すなわち，読出されたワードから論理信号形式の２進情報を取り出すこと（ワードのメモリセルは，直接使用可能な論理情報要素を必ずしも記憶しておらず、一般的には、例えば差動増幅器よりなる適切な回路によって論理信号に変換される変更可能な物理的特性を有している）。

【０００８】標準的方法では、或る数のビットに符号化されているアドレスが、シフトレジスタによってシリアルに受けられる。この方法は、受けられるアドレスビットと同じ数の多くのクロック信号サイクルだけ続く。

【０００９】最大許容アクセス時間は，クロック信号の半サイクルの奇数倍の持続期間としばしば等しい。例えば，このアクセス時間は，メモリがマイクロワイヤまたはＩ２Ｃ型バスに接続されている場合には３半サイクルに設定され、メモリがＳＰＩバスに接続されている場合には半サイクルに設定される。

【００１０】従って、メモリが他の装置と通信するバス

の形式が、所与のクロック信号周波数に対して，最大許容アクセス時間を決定する。例えば，ＳＰＩバスと２ＭＨｚのクロック信号周波数とを使用したい場合には、許容アクセス時間は２５０ナノ秒に制限され，これは高速パラレルアクセスメモリを読出す装置の性能レベルに近い性能レベルに対応する。

【００１１】必要な切換え速度に固有な構造に技術的困難が生ずる。解決手段があるとすれば，使用される回路は，高電力消費回路であることが多い。これは最小電力消費レベルが求められる携帯用にしばしば構成されるメモリには、ほとんど望ましくない。実際に、そのため、使用されるバスの形式と期待される最大許容アクセス時間に対してクロック信号の周波数が決定される。

【００１２】

【発明が解決しようとする課題】本発明の目的は，上記した技術的問題を解決して，技術的簡潔さと低電力消費とを併せ持ち，外部から見たとき、従来のシリアルアクセスメモリの標準的な構成と標準的な読出し方法と機能的に同様な、シリアルアクセスメモリの構成と読出し方法を提供することである。

【００１３】

【課題を解決するための手段】各メモリが複数ワードにマトリクスの形に構成されており、各ワードの内容が２進情報要素を表し、各ワードがｋビットに２進モードで符号化されたアドレスでアクセスでき（ｋは１より大きい整数）、アドレスビットがアドレス入力端子を介してメモリにシリアルに供給される、集積回路メモリのワードの内容を読出す本発明による方法は，１ワードの内容を読出すために，読出したい１ワードのアドレスの初めのｑビットをシリアルに受けて（ｑはｋより小さい整数），前記アドレスの残りの〔ｋ－ｑ〕ビットを受けることと並行して，前記受けたアドレスの前記初めのｑビットを復号し，前記受けたアドレスの前記初めのｑビットに対応する初めのｑアドレスビットを有するワードに読出し回路を接続し、前記ワードの内容が表す２進情報要素を取り出し，読出したい１ワードの前記アドレスの前記残りの〔ｋ－ｑ〕ビットを復号すると共に，前記受けたアドレスの前記初めのｑビットに対応するアドレスビットを有する前記ワードの前記内容が表す前記２進情報要素を、メモリのデータ出力端子に出力する。

【００１４】従って、本発明は，アドレスビットがまだすべて受けられていない内に，アドレス復号と読出しを開始することを提案する。従って、内部的な増強は、クロック信号の半サイクル数の見地から，最大許容内部アクセス時間（すなわち、アドレス復号とワードの読出しの最大時間）で達成され，メモリの外部からみて，最大許容アクセス時間は、所与の周波数に対して、同じままである。そのため、外部からみたアクセス時間は，アドレス復号と読出し動作の実行期間によってはもはや決定されず、その実行期間より小さい。そのため、これによ

り．最大アクセス時間を同一として場合、許容クロック信号周波数を増大できる。同時に、復号が、アドレスビットがまだすべて受けられていない内に、開始するので．復号の開始時に、受けたビットに対応するアドレスビットを有するワードの全てから情報を取り出すために．数個の読出し回路が並列して作動される。出力から出力される情報は、アドレス全体がわかったときに、選択される。そこで、本来の復号と読出しの動作と比較して短時間の簡単な再経路指定が行われ．アクセス時間は．主として．読出し増幅器の使用等同様な動作の遅さにより制限される。

【００１５】更に本発明によれば、複数ワードに構成されており、各ワードの内容が２進情報要素を表し．各ワードが、ｋビットに２進モードで符号化されたアドレスでアクセスできる（ｋは１より大きい整数）、集積回路メモリであって．アドレスビットをシリアルに受けるアドレス入力端子と、アドレスされたワードの内容に対応する２進情報要素を出力するデータ出力端子と．受けたアドレスビットを記憶する入力レジスタと、受けたアドレスビットを復号する回路と、ワードを読出す回路に接続する回路とを具備している集積回路メモリにおいて、前記ワードが．複数のワード群に構成されており．各ワード群に含まれるワードの初めのｋアドレスビットが互いに異なり、残りの〔ｋ－ｑ〕アドレスビットが同一であり（ｑはｋより小さい整数）、各ワード群ごとに読出し回路が設けられ、メモリがｋアドレスビットを受けると．受けた初めのｋアドレスビットに対応するワード群の内容により表される２進情報を前記読出し回路が取り出し．メモリが更に、受けたｋビットに対応するアドレスを有するワードの内容により表される２進情報を、前記データ出力端子に出力する制御出力マルチプレクシング回路を具備している。

【００１６】上記したメモリは、上記した方法を実施する。標準的なメモリと比較すると、本発明によるメモリは．並列に動作する数個の読出し回路が存在するために．寸法がわずかに大きくなる。しかし、注目すべきは．動作が全体として標準的なメモリの動作と同様なこのメモリの技術的単純性である。許容クロック信号周波数を高くするために、標準的なメモリと同じ形式の読出し回路を使用できる。これは、消費電力の増大が．使用される読出し回路の数が増大することのみによるものであり．メモリの回路の複雑さが増したことによるものではないことを意味する。

【００１７】実際に、読出したいワードのアドレスの内の初めのｑビットの復号は．標準的な行デコード回路及び列デコード回路で実施できる。受けた残りの〔ｋ－ｑ〕ビットの復号は、マルチプレクシング回路と読出し回路のための制御信号の発生に対応する。

【００１８】標準的なメモリにおいて．受けたアドレスビットは、ｋ個のセルから形成されるシフトレジスタに

記憶される。このシフトレジスタは．アドレス入力端子に接続される。シーケンシャル読出しモードで動作可能なメモリのため．この入力レジスタは更に、２進アドレスカウンタとして動作できるように構成される。

【００１９】好ましい態様において．本発明は．第１に．初めのｑアドレスビットの、第２に、残りの〔ｋ－ｑ〕アドレスビットを記憶する。従って、それぞれｑセルと〔ｋ－ｑ〕セルを有する２つのシフトサブレジスタが使用される。２つのサブレジスタはアドレス入力端子に接続される。この構成により、常に同じセルに同じ行のアドレスビットの記憶が可能となる。これにより本発明が容易に実施できる。事実、第ｑ番目のビットが受けたとすぐに初めのｑアドレスビットを供給するように単一シフトレジスタを使用することは．さらに複雑になる。単一シフトレジスタを使用する場合、復号を行いながら．シフトによって、このレジスタのセルの内容を変更することになる。実際に．そのため．復号のために使用されるｑビットの安定性を確保するため、入力レジスタと復号回路との間にバッファレジスタを設けることが必要である。

【００２０】さらにまた．ｑセルを有し、アドレス入力端子に直接接続された単一シフトレジスタ型の入力レジスタに動作を限定することはできない。第１に．アドレスの復号のために使用されるビットの安定性を確保するため．受けた初めのｑアドレスビットを記憶できることが必要である。第２に、明確（ｋ－ｑ＞１であれば）かつ安定な方法で出力マルチプレクシング回路を制御できるようにするため、受けた残りの〔ｋ－ｑ〕アドレスを記憶できることも必要である。

【００２１】好ましい態様において．本発明は．第１のアドレスに対応する第１のワードの内容の読出し後、メモリの第２のワードの内容により表される第２の２進情報要素をメモリがデータ出力端子に自動的に出力するようないわゆるシーケンシャル読出しモードをメモリが有する方法を提供する。

【００２２】シリアルアクセスメモリは、外部から受けたアドレスがアドレスカウンタに格納され、その受けたアドレスに対応する情報が外部に出力されるとすぐに、格納されたアドレスが自動的に変更されて、外部の介在なしに、その後に続くワードの内容に対応する情報要素が自動的に出力されるような読出しモードを有する。実際．アドレスの変更は、アドレスのインクリメントが最も普通である。

【００２３】同時に、本発明は、入力レジスタがは、２進アドレスカウンタである．メモリを提供する。

【００２４】勿論、標準的なメモリの場合とは異なり、シーケンシャル読出しモードでは、初めのｑアドレスビットに対応するサブレジスタのｑセルの内容の方法上の変更はない。これら内容は．第２のワードが第１のワードとは異なる初めのｑアドレスビットを有しない限り、

変更されない。格納された残りの〔ｋ－ｑ〕ビットは初めのｑアドレスビットの変更が必要かどうかを判別するために使用される。

【００２５】

【発明の実施の形態】図１と図２は、例えば、周知の半導体技術により製造されたＥＥＰＲＯＭ型メモリである。メモリ１を示す。

【００２６】例えば、このメモリ１は、各ワードがｂ個の基本メモリセルにより形成されるｍワード（Ｗ０からＷ２５５）から各行が構成された１行に構成されている。

【００２７】標準的な方法では、ｌ．ｍ，ｂは２の幂と等しい整数となる。以下、説明において、ｌ＝ｍ＝２４＝１６、およびｂ＝２３＝８とする。

【００２８】各ワードごとに、典型的に、２ｐ＝ｌ＊ｍを満足するｋビットに符号化されたアドレスＡＤＤが与えられる。以下の説明において、ｋ＝８とし、アドレスの上位４ビットが、選択したい行を決定し、アドレスの下位４ビットが、その選択したい行において読出したいワードを決定すると理解されたい。

【００２９】本発明によれば、この方法は、アドレスＡＤＤの初めのｑ（＝ｋ－ｐ）ビットを受けた時に、そのアドレスＡＤＤの復号を開始する。ここで、ｑとｐは整数であり、ｐ＜ｋである。メモリには２ｐワードがある。ｑアドレスビットに対して、受けたこれらｑアドレスビットと初めのｑアドレスビットが同じアドレスを有するワードは、２ｐワードある。従って、受けた初めのｑアドレスビットに基づいて、２ｐ個の２進情報要素が取り出される。

【００３０】そのため、ワードは、２ｐワード群に分けられ、各ワード群は次のように読出し回路が設けられる。各ワード群において、ワードは、初めのｑアドレスビットが互いに異なる、ワードは、残りのｐアドレスビットが同一である。実施例において、ｐは１と等しくなっている。

【００３１】従って、アドレスＡＤＤをシリアルに受けたとすると、このアドレスの復号は、最下位ビットがまだ入力に現れないうちに開始する。これは、この条件において、受けた初めのビットに基づいて、選択すべき行を確実に決定できる一方、読出したい特定のワードに関しては、或る程度の不確実さが残ることを意味する。ｐ＝１の場合、メモリは、２つの半（メモリ）アレイＭ１とＭ２により形成され、半アレイＭ１は、例えば、最後のアドレスビットが１と等しいメモリ空間に対応し、他方の半アレイＭ２は、最後のアドレスビットが０と等しいメモリ空間に対応すると考えられる。メモリアレイは、偶数パリティ半アレイと奇数パリティ半アレイとに分けられる。

【００３２】メモリ１は、読出したい１つのワードのアドレスＡＤＤをシリアル受けるアドレス入力端子２と、

アドレスビットを受ける入力レジスタＲＩと、受けたアドレスＡＤＤに対応する２進情報要素ＤＡＴＡを、標準的な方法で、外部に、シリアルに出力するデータ出力端子３と、メモリの外部で発生し、メモリ１の動作速度を設定するクロック信号ＣＬＫを受ける入力端子４と、読出し制御論理信号ＲＥＡＤを受ける入力端子５（１例では、ＲＥＡＤ＝１の時、メモリのワードが読出される）と、各半アレイの１行のうち１行を選択する行デコード回路ＬＤ、２つの（すなわち、２ｐ）マルチプレクサＭＵＸ１とＭＵＸ２を制御して、これらマルチプレクサによって、半アレイ毎に、行デコード回路により選択された行の内の読出すべき１ワードを選択する列デコード回路ＣＤとを具備している。

【００３３】メモリ１は、更に、クロック信号ＣＬＫと読出し制御信号ＲＥＡＤを受けて、メモリ１の動作を適切に同期させる制御信号をメモリ内の様々な回路に送る制御回路ＣＣと、選択された２つのワードから２つの２進データ素子を取り出すため、半アレイＭ１とＭ２の１つにそれぞれ１つが付属した、２つの読出し回路ＳＡ１とＳＡ２と、取り出された２ｐ２進情報要素の１つを（制御回路ＣＣから受けた選択信号の状態に従って）選択して、その取り出し選択した情報要素を外部に出力するための、２ｐパラレル入力と１つのパラレル出力とを有する出力マルチプレクサＭＵＸＳと、出力レジスタＲＯとを備える。典型的に、この出力レジスタは、パラレル入力／シリアル出力のシフトレジスタである。出力レジスタＲＯの入力は、出力マルチプレクサＭＵＸＳの出力に接続され、出力レジスタＲＯの出力は、出力端子３に接続されている。（情報要素がｂ＝８ビットに符号化されているとの）上記条件によれば、この出力レジスタＲＯは、当然、８つのセルにより形成されている。

【００３４】以下の動作の説明に基づいて当業者は格別の問題なく回路を製造できるので、回路の論理構成の詳述は省略する。

【００３５】入力レジスタＲＩは、次の２つのレジスタにより形成される。すなわち、受けたアドレスＡＤＤの初めのｑビットを格納するシリアル入力とパラレル出力を有する第１のサブレジスタＲＩ１と、受けたアドレスＡＤＤの残りの〔ｋ－ｑ〕ビットを格納するシリアル入力とパラレル出力を有する（セル１つのみにより形成される）第２のサブレジスタＲＩ２とにより形成されている。

【００３６】２つのサブレジスタＲＩ１とＲＩ２は、それぞれ入力をアドレス入力端子２に接続したシフトレジスタである。

【００３７】サブレジスタＲＩ１のパラレル出力は、デコード回路ＬＤとＣＤに接続されている。サブレジスタＲＩ１のセルの内の４つは、行デコード回路ＬＤに接続され、他の３つのセルは、列デコード回路ＣＤに接続される。なお、同等な容量を有する標準的なメモリと比較

して．列デコード回路は．４ビットではなく３ビットを処理するため．サイズが小さいことに注目されたい。

【００３８】サブレジスタＲｉ１は．シフト制御論理信号ＳＲ１を受ける。ＳＲ１＝１のとき．セルの内容は．クロック信号の前縁に応答して１セルづつシフトされる。

【００３９】サブレジスタＲｉ２のパラレル出力（本実施例の場合、ｋ－ｑ＝１であるからシリアル出力である）は、制御回路ＣＣに接続される。ＡＤＯはサブレジスタＲｉ２の内容である。サブレジスタＲｉ２は．シフト制御論理信号ＳＲ２を受ける。ＳＲ２＝１のとき、セルの内容は、クロック信号の前縁に応答して１セルづつシフトされる。

【００４０】シーケンシャル読出しモードを持たないメモリ（図１に示す場合）

初めのｑアドレスビットを受けると．これらビットはサブレジスタＲｉ１に格納される。

【００４１】残りのｐアドレスビットを受けると．これらビットはサブレジスタＲｉ２に格納される。このとき．制御信号ＳＲ１は、０と等しい状態に保持されて、サブレジスタＲｉ１の内容が変更されないようにする。

【００４２】ワードの読出しは、つぎの段階からなる。

① 読出したいワードの初めの７アドレスビットを第１のサブレジスタＲｉ１にシリアルに受けて格納する（ＳＲ１＝１）。

② 最後のアドレスビットを第２のサブレジスタＲｉ２のセルに受けて格納する（ＳＲ２＝１とＳＲ１＝０）ことと並行して．受けた初めの７アドレスビットを行デコード回路ＬＤと列デコード回路ＣＤにより復号し．受けた初めの７アドレスビットに初めの７アドレスが一致する．２つの半アレイＭ１とＭ２の内のワードに読出し回路ＳＡ１とＳＡ２をそれぞれ接続し．それら２つのワードにより表される２進情報要素を、読出し回路ＳＡ１とＳＡ２によって取り出し．

③ 制御回路ＣＣによって残りのアドレスビット（ＡＤＯ）を復号し（すなわち．出力マルチプレクサに与えられる選択信号を発生し）．受けた８アドレスビットに一致するアドレスを有するワードの内容によって表される２進情報要素を．出力マルチプレクサＭＵＸＳと出力レジスタＲＯによって出力データ端子３に出力する。実際には．ｐ＝１であるので．出力マルチプレクサＭＵＸＳの制御入力にサブレジスタＲｉ２の出力を接続すること＊によって、出力マルチプレクサＭＵＸＳを直接制御することができる。

【００４３】図１に示す実施例は、１つの例として説明されている。事実、市販のシリアルアクセスメモリのほとんどは、シーケンシャル読出しモードで動作する。

【００４４】シーケンシャル読出しモードを持つメモリ（図２に示す場合）

図１と比較して．つぎのような違いがある。メモリは、シーケンシャル読出しモードに入ることができる制御論理信号ＳＲを受ける制御入力端子６を有する。ＳＲ＝１がシーケンシャル読出しモードに対応するものとする。入力レジスタＲＩは２進アドレスカウンタとして動作する。第１と第２のサブレジスタＲｉ１．Ｒｉ２は単なるシフトレジスタではない。シーケンシャル読出しモードは．サブレジスタＲｉ１．Ｒｉ２の内容がメモリ内部で変更できることを想定している。入力レジスタＲＩは（制御論理信号ＩＮＣによって）制御回路ＣＣにより制御され、（例えば、信号ＩＮＣが論理状態１であれば）前記カウンタの内容を（典型的にはインクリメント１で）自動変更する。

【００４５】サブレジスタＲｉ１、ＲＩ２は、制御論理信号ＩＮＣを受けて、（例えば、制御論理信号の前縁に応答して）その内容を１単位インクリメントする。

【００４６】さらにまた．サブレジスタＲｉ２は．桁上がり論理信号ＣＲｉ２を出力する１つの出力を有する。この信号ＣＲＩ２は、サブレジスタＲＩ２の内容のインクリメントの後このレジスタに格納されたすべてのビットはゼロ（０）であるとき．所定の状態、例えば．状態１となる。これは、インクリメント前．このレジスタに格納されるすべてのビットが１である場合に対応する。一般に、これは．インクリメント前に読み取ったワードのアドレスの次のアドレスにあるワードを読出したい場合は．サブレジスタＲｉ１の内容を変更する必要があることに相当する。したがって、信号ＩＮＣに加え．信号ＣＲＩ２がサブレジスタＲＩ１に与えられ、．同時にＩＮＣとＣＲｉ２＝１のときだけ、ＩＮＣとＣＲＩ２＝１の前縁に応答して、サブレジスタＲＩ１の内容がインクリメントされる。読出し回路ＳＡ１とＳＡ２は各々、それぞれＲＥＡＤ１とＲＥＡＤ２で表す読出し制御信号を受ける。

【００４７】次のようにする：

$$READ1 = SR*READ*AD0 + READ*/SR$$

$$READ2 = SR*READ*/AD0 + READ*/SR$$

＊は論理積を表し、＋は論理和を表し．／は反転信号を表す。

【００４８】アドレスからの情報の取り出しに関し、アドレスが、アドレス入力端子２によりメモリに与えられるか．内部で発生するかにより、２つのケースに分けることができる。

【００４９】１　アドレスを外部から受ける場合

この例は図１に示す動作と同様な動作態様に相当する。

【００５０】ワードを読出すには、図１に示す例と同様な方法で、初めのｑビットは行デコードと列デコード回路ＬＤ、ＣＤにより使用され、残りのｐビットは制御回路ＣＣにより使用される。

【００５１】メモリセルから取り出された2^nの情報要素が読出されると（もちろん、ＲＥＡＤ１＝ＲＥＡＤ２＝ＲＥＡＤである）、受けたｋビットに対応する情報が出力マルチプレサーＭＵＸＳ（ＡＤＤによる選択）によって出力レジスタＲＯに格納される。ついで、出力レジスタＲＯにおけるシフトによって、情報要素はデータ出力端子に出力される。

【００５２】２　シーケンシャル読出し

シーケンシャル読出しモードにおいて、最初に与えられたアドレスに対応する情報要素の出力に続いて、アドレスは、他の情報要素を外部に連続的に出力するように、外部からの介在なしに、変更される。

【００５３】従来のように、上記した最初のアドレスは、次のアドレスにあるワードに格納されている情報を与えるため、１単位インクリメントされるとする。

【００５４】つぎの段階が行われる。

①　ｋアドレスビットを外部から受けて、対応する情報をデータ出力端子に出力する。

②　データ出力端子への情報の出力と並行して、第２のサブレジスタＲＩ２の内容を１単位インクリメントし、第１のサブレジスタＲｉ１を（ＣＲＩ２の関数としての）条件付きでインクリメントし、インクリメント後、サブレジスタＲＩ１の内容を復号し、

③　ＲＥＡＤ１とＲＥＡＤ２の状態を決定する。インクリメント後のサブレジスタＲｉ２の内容ＡＤＯの関数として適切な読出し回路ＳＡ１またはＳＡ２によって所望情報を取り出す。

【００５５】例えば、出力レジスタに記憶されている情報ビットの半分がデータ出力端子に実際に出力されていると、インクリメントをすることができる。意義なことは、出力レジスタの最終ビットの出力を待って、次の読出し動作を行う必要がないことである。これが最大許容クロック周波数を効果的に下げることなる。言い換えれば、シーケンシャル読出しモードにおいても、非シーケンシャル読出しモードの場合（または、正確には、アドレスが外部からり与えられる場合）の内部アクセス時間と少なくとも等しい内部アクセス時間の利益が得られる利点がある。

【００５６】図示した例において、半アレイの第１のワードの第１のアドレス（ＡＤＯが０へ）を外部から受けた仮定する。この第１のアドレスのインクリメント（ＡＤＯが１へ）は、半アレイＭ１にある第２のワードの第２のアドレスを与える。第１、第２のアドレスの初めのｑビットは同一である。第２のワードの内容を読出すために、サブレジスタＲｉ１に格納されているｑビットは変更されない（ＣＲＩ２＝０）。ＲＥＡＤ１＝／ＲＥＡＤ２＝１である。

【００５７】半アレイＭ２にある次のワードを読出すために、下記の段階が行われる。

①　制御信号ＩＮＣによって、サブレジスタＲＩ２（ＡＤＯ＝０とＣＲＩ２＝１）の内容をインクリメントし、サブレジスタＲＩ１（第ｑ番目のアドレスビットと、おそらく他のアドレスビットの内の１つ以上のビットの変更）の内容をインクリメントし、

②　インクリメント後サブレジスタＲＩ１に格納されているｑビットをデコード回路ＬＤとＣＤによって復号し、

③　読出し回路ＳＡ２（ＲＥＡＤ２＝／ＲＥＡＤ１＝１）によって、インクリメント後のアドレスに対応するワードを読出し、

④　出力レジスタに、取り出した２進情報を格納し、

⑤　情報を出力する。

【００５８】勿論、本発明は、上記の実施例に限定されるものではなく、他の改良及び拡張を、本発明の精想から逸脱することなく行うことができる。特に、メモリセルは３以上の多数の群に構成できる。この場合、メモリ内部でみたアクセス時間は増大し、消費電力もメモリの占有スペースも対応した増大する。

【００５９】さらにまた、2^n出力レジスタを使用し、その各々に読出し回路の１つを付属させ、出力マルチプレクサをこれら出力レジスタとデータ出力端子間に設けること可能である。その時、シーケンシャル読出しモードで、常に、2^nワードを読出し、データ出力端子にこれらワードの連続に出力することができる。従って、初めのｑアドレスビットを変更しない限り、効果的な読出しはできない。

【図面の簡単な説明】

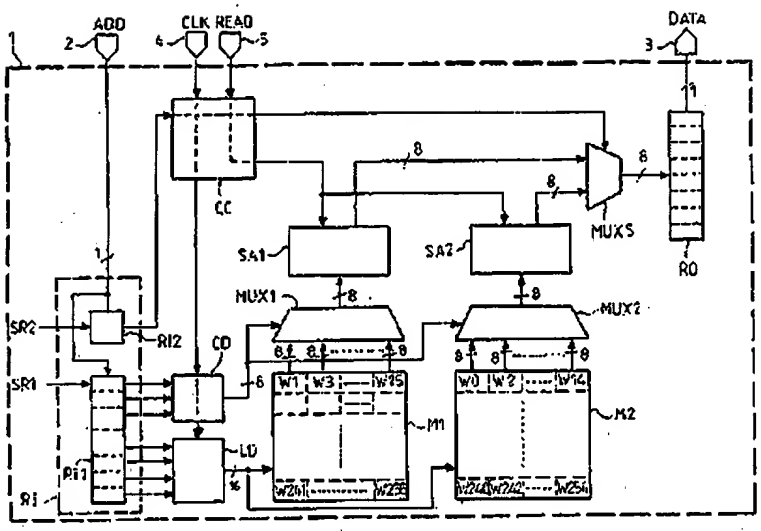
【図１】　本発明によるメモリ構成を示す。

【図２】　シーケンシャル読出しモードを使用できる、本発明による他のメモリ構成を示す。

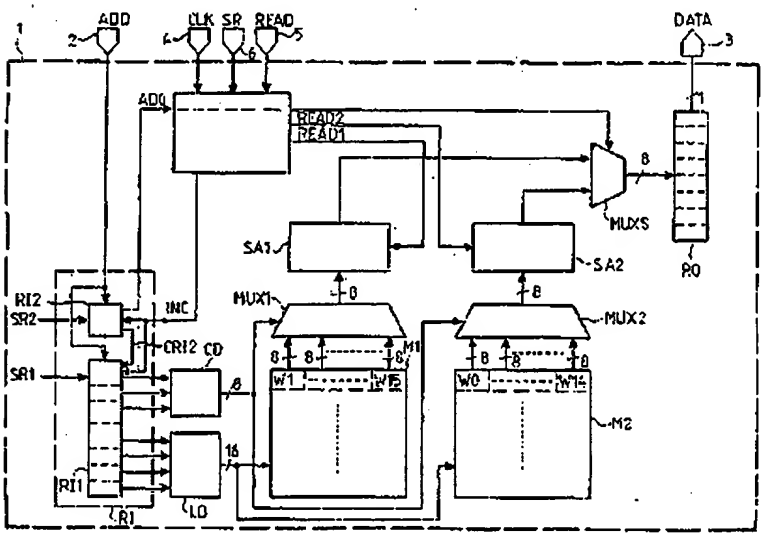
【符号の説明】

１　メモリ
２　アドレス入力端子
３　データ出力端子
４．５　入力端子
６　制御入力端子
ＲＩ　入力レジスタ
ＬＤ　行デコード回路
ＣＤ　列デコード回路
ＳＡ　読出し回路
ＭＵＸＳ　出力マルチプレクサ
ＲＯ　出力レジスタ

【図1】


ADD
CLK
READ
DATA
CC
SA1
SA2
MUXS
RO
MUX1
MUX2
SR2
RI2
CD
SR1
RI1
RI
LD
M1
M2
W1
W3
W15
W0
W2
W14

【図2】


ADD
CLK
SR
READ
DATA
ADD
READ2
READ1
SA1
SA2
MUXS
RO
MUX1
MUX2
RI2
SR2
INC
CRI2
CD
SR1
RI1
RI
LD
M1
M2
W1
W15
W0
W14

CLAIMS

[Claim(s)]

[Claim 1] Each memory is constituted by two or more words at the form of a matrix, and the contents of each WORD express a binary information element. Each WORD can access in the address encoded by k bits in binary mode (k is a larger integer than 1). In order that an address bit may be the approach of reading the contents of the WORD of integrated-circuit memory by which it is serially supplied to memory through an address input terminal and may read the 1-word contents Are concurrent with receiving serially the first q bits of the 1-word address to read (q being an integer smaller than k), and receiving the remaining [k-q] bits of said address. Decode the first [said] q bits of said received address, and a read-out circuit is connected to the WORD which has the first q address bit corresponding to the first [said] q bits of said received address. Take out the binary information element which the contents of said WORD express, and while decoding said remaining [k-q] bits of said 1 word [to read] address How to read the contents of the WORD of the integrated-circuit memory characterized by outputting said binary information element which said contents of said WORD which has an address bit corresponding to the first [said] q bits of said received address express to the data output terminal of memory.

[Claim 2] Memory is an approach according to claim 1 characterized by having the sequential read-out mode which outputs automatically the 2nd binary information element expressed according to the word [2nd] contents of memory after read-out of the contents of the 1st WORD corresponding to the 1st address to a data output terminal.

[Claim 3] The approach according to claim 2 characterized by carrying out while outputting the binary information expressed according to the word [1st] contents in decode of the address of the 2nd WORD to the data output terminal.

[Claim 4] An approach given in either of claims 2-3 characterized by taking out one binary information element at once in sequential read-out mode.

[Claim 5] It is constituted by two or more words and the contents of each WORD express a binary information element. The address input terminal which each WORD can access in the address encoded by k bits in binary mode (k is a larger integer than 1) and which is integrated-circuit memory and receives an address bit serially, The data output terminal which outputs the binary information element corresponding to the contents of the WORD by which the address was carried out, In the integrated-circuit memory possessing the input register which memorizes a carrier beam address bit, the circuit which decodes the received address bit, and the circuit linked to the circuit which reads WORD Said WORD is constituted by two or more WORD groups, and the first k address bits of the WORD contained in each WORD group differ mutually. If the remaining [k-q] address bits are the same (q is an integer smaller than k), a read-out circuit is prepared for every WORD group and memory receives k address bit Said read-out

circuit takes out the binary information expressed according to the contents of the WORD group corresponding to the first k address bit of a carrier beam. Integrated-circuit memory characterized by providing the control-output multiplexing circuit where memory outputs the binary information expressed according to the contents of the WORD which has the address corresponding to received k bits further to said data output terminal.
[Claim 6] An input register is memory according to claim 5 characterized by being constituted with two shift subregisters formed from q cels and the cel of the [k-q] individual, respectively.
[Claim 7] An input register is memory according to claim 6 characterized by being a binary address counter.
[Claim 8] A control circuit is memory according to claim 7 characterized by having a means to change the contents of the input register.
[Claim 9] Memory given in any 1 term of claims 5-8 characterized by having the output register connected to the read-out circuit since the binary information element taken out by the read-out circuit is stored.
[Claim 10] Memory given in any 1 term of claims 5-9 characterized by being electrically programmable and being eliminable memory.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to serial access memory. Although especially this invention can be adapted for memory volatile [of other formats], or non-volatile, it relates to eliminable programmable read-only memory (EEPROMs) electrically.
[0002]
[Description of the Prior Art] (from a number of an information element of standpoints memorized) Current development of the memory of the integrated-circuit format of having a very large information storage capacity is furthered by the request which wants to make high the frequency of the clock signal which determines the working speed of the system incorporating these integrated-circuits memory. Consequently, coincidence also has the research which shortens increasingly time amount which accesses the contents of the WORD which constitutes these memory. "WORD" means a physical stereo with the contents showing the binary information element encoded by b bits here. b is an integer here. WORD is formed of b basic memory cells, and each basic memory cell is typically formed of a store circuit.
[0003] Seeing from the access time, parallel access memory is the most advantageous memory. The period corresponding to 1 cycle of the clock signal which determines the working speed of such memory is enough to give one of the memory of these for the one address which is the WORD from which the contents are read in parallel.
[0004] Nevertheless, as for serial access memory, that a manufacture price is low, that a package is especially small light clearly, etc. have a clear advantage again as compared with parallel access memory. In fact, there are very few contact pins which need serial memory. The number of contact pins of an integrated circuit affects extremely the amount of space which an integrated circuit occupies. Consequently, serial access memory is very useful portable.
[0005] However, it is desirable that the clock signal frequency and storage capacity of these

serial access memory can be increased. Memory capacity is 64 kilobits and the present most highly efficient product operates on the frequency of about 1MHz. The frequency more than the storage capacity and the 5MHz range of about 256 kilobits is expectable in the near future.
[0006] In fact, the technical issue essentially involved to the access time to the contents of WORD in read-out mode produces increase of the clock signal frequency of these memory. With the "access time" in "read-out mode" The time of the address of WORD being known by memory (at namely, the time of memory receiving all the address bits of WORD serially), The time of the binary information which the contents of the memory cell of WORD express beginning to become available (when memory being serial output memory), Or please understand that the period seen in the exterior during the time of becoming available in the exterior of memory through one or more output pins is meant (when memory is parallel output memory or the information element is encoded by 1 bit).
[0007] The access time is essentially restricted by time amount required to perform the following two phases in order.
- Switch appropriately various change equipments for connecting a read-out circuit to the WORD which has decoding the address which memory received, i.e., the contents showing binary information reading.
- The binary information on a logic signal format is taken out from an original read-out process, i.e., the read WORD, (the memory cell of WORD does not necessarily memorize a directly usable logic information element, but, generally the metaphor has the physical characteristic which is changed into a logic signal by the suitable circuit which consists of differential amplifier and which can be changed).
[0008] By the standard approach, the address encoded by the bit of a certain number can receive serially with a shift register. Only many clock signal cycles of the number as the address bit which can be received with this same approach continue.
[0009] The maximum-permissible access time is often equal to an odd times as many duration as the half cycle of a clock signal. For example, this access time is set as 3 half cycles, when memory is connected to the micro wire or the I2C mold bus, and when memory is connected to the SPI bus, it is set as a half cycle.
[0010] Therefore, the format of a bus that memory communicates with other equipments determines the maximum-permissible access time to a given clock signal frequency. For example, the permission access time is restricted to 250 nanoseconds and this corresponds to the engine-performance level near the engine-performance level of the equipment which reads high-speed parallel access memory to use an SPI bus and the clock signal frequency of 2MHz.
[0011] Technical difficulty arises in structure peculiar to a required toggling speed. If there is a solution means, the circuit used is a high power consumption circuit in many cases. In the memory often constituted by portable [which is asked for the minimum power consumption level], this is hardly desirable. The frequency of a clock signal is determined to the maximum-permissible access time it is expected in fact therefore that is the format of the bus used.
[0012]
[Problem(s) to be Solved by the Invention] The purpose of this invention is offering the standard configuration of the conventional serial access memory, the standard read-out approach, the same configuration of serial access memory as a functional target, and the read-out approach, when the above-mentioned technical issue is solved, and it has technical conciseness and low power consumption and they are seen from the outside.
[0013]

[Means for Solving the Problem] Each memory is constituted by two or more words at the form of a matrix, and the contents of each WORD express a binary information element. Each WORD can access in the address encoded by k bits in binary mode (k is a larger integer than 1). The approach by this invention which reads the contents of the WORD of integrated-circuit memory that an address bit is serially supplied to memory through an address input terminal Are concurrent with receiving serially the first q bits of the 1-word address to read (q being an integer smaller than k), and receiving the remaining [k-q] bits of said address, in order to read the 1-word contents. Decode the first [said] q bits of said received address, and a read-out circuit is connected to the WORD which has the first q address bit corresponding to the first [said] q bits of said received address. Take out the binary information element which the contents of said WORD express, and while decoding said remaining [k-q] bits of said 1 word [to read] address Said binary information element which said contents of said WORD which has an address bit corresponding to the first [said] q bits of said received address express is outputted to the data output terminal of memory.

[0014] Therefore, before the address bit has received this invention altogether yet, it proposes starting address decode and read-out. Therefore, internal enhancement is attained from the standpoint of the number of half cycles of a clock signal in the interior access time of the maximum permissible (namely, the maximum time amount of read-out of address decode and WORD), and the maximum-permissible access time is still the same to a given frequency seen from the exterior of memory. Therefore, the access time seen from the outside is not determined any longer depending on the activation period of address decode and read-out actuation, but is smaller than the activation period. therefore -- being the same in the maximum access time by this -- carrying out -- a case -- a permissible clock signal frequency -- it can increase . Since it starts to coincidence before the address bit has received all for decode yet, in order to take out information from all the WORD that have an address bit corresponding to the received bit, to it, some read-out circuits stand in a row and operate at the time of initiation of decode. The information outputted from an output is chosen when the whole address is found. Then, easy short-time re-routing is performed as compared with original decode and actuation of read-out, and the access time is mainly restricted by the lateness of the same actuation as use of a sense amplifier etc.

[0015] Furthermore, according to this invention, it is constituted by two or more words and the contents of each WORD express a binary information element. The address input terminal which each WORD can access in the address encoded by k bits in binary mode (k is a larger integer than 1) and which is integrated-circuit memory and receives an address bit serially, The data output terminal which outputs the binary information element corresponding to the contents of the WORD by which the address was carried out, In the integrated-circuit memory possessing the input register which memorizes a carrier beam address bit, the circuit which decodes the received address bit, and the circuit linked to the circuit which reads WORD Said WORD is constituted by two or more WORD groups, and the first k address bits of the WORD contained in each WORD group differ mutually. If the remaining [k-q] address bits are the same (q is an integer smaller than k), a read-out circuit is prepared for every WORD group and memory receives k address bit Said read-out circuit takes out the binary information expressed according to the contents of the WORD group corresponding to the first k address bit of a carrier beam. The control-output multiplexing circuit where memory outputs the binary information expressed according to the contents of the WORD which has the address corresponding to received k bits further to said data output terminal is provided.

[0016] The above-mentioned memory enforces the above-mentioned approach. Since some read-out circuits where the memory according to this invention as compared with standard memory operates to juxtaposition exist, a dimension becomes large slightly. however -- it should observe -- actuation is the technical simplicity of the same memory of this as actuation of memory standard as a whole. In order to make a permissible clock signal frequency high, the read-out circuit of the same format as standard memory can be used. This means that increase of power consumption is not what depends only on the number of the read-out circuits used increasing, and is depended on what the complexity of the circuit of memory increased.
[0017] q-bit decode of the start of the addresses of WORD to read can actually be carried out in a standard line decoding circuit and a train decoding circuit. Decode of the [k-q] bit of the carrier beam remainder corresponds to generating of the control signal for a multiplexing circuit and a read-out circuit.
[0018] The received address bit is memorized in standard memory by the shift register formed from k cels. This shift register is connected to an address input terminal. For the memory which can operate in sequential read-out mode, further, this input register is constituted so that it can operate as a binary address counter.
[0019] In a desirable mode, this invention memorizes [1st] the remaining [k-q] address bits to the 2nd of the first q address bit. Therefore, two shift subregisters which have q cel and the [k-q] cel, respectively are used. Two subregisters are connected to an address input terminal. By this configuration, it becomes memorizable [the address bit of the same line as the always same cel]. Thereby, this invention can carry out easily. In fact, it becomes still more complicated to use a single shift register so that the first q address bit may be supplied shortly after the q-th bit won popularity. When using a single shift register, the contents of the cel of this register will be changed by shift, decoding. In order to secure the stability of q bits used for decode in fact therefore, it is required to prepare a buffer register between an input register and a decoder circuit.
[0020] It has q cel and actuation cannot be limited to the input register of the single shift register mold by which direct continuation was carried out to the address input terminal further again. In order to secure the stability of the bit used [1st] for decode of the address, it is required for the received first q address bit to be memorizable. In order to enable it to control an output multiplexing circuit to the 2nd by the clear (k-q> if it to be 1) and stable approach, it is required for it for the received remaining [k-q] address to be also memorizable.
[0021] In a desirable mode, this invention offers how memory has the so-called sequential read-out mode in which memory outputs automatically the 2nd binary information element expressed according to the contents of the 2nd WORD of memory to a data output terminal after read-out of the contents of the 1st WORD corresponding to the 1st address.
[0022] The stored address is changed automatically and serial access memory has without external mediation read-out mode with which the information element corresponding to the contents of the WORD which continues after that is outputted automatically, shortly after the address received from the exterior is stored in an address counter and the information corresponding to the received address is outputted outside. Modification of the address actually has the most common increment of the address.
[0023] This invention provides coincidence with the memory whose input registers are ** and a binary address counter.
[0024] Of course, unlike the case of standard memory, there is no modification on the approach of the contents of the q cel of the subregister corresponding to the first q address bit with

sequential read-out mode. These contents are not changed unless it has the first q address bit in which the 2nd WORD differs from the 1st WORD. The stored remaining [k-q] bits are used in order that modification of the first q address bit may distinguish whether it is the need.
[0025]
[Embodiment of the Invention] Drawing 1 and drawing 2 show the memory 1 which is the EEPROM mold memory manufactured by well-known semiconductor technology.
[0026] For example, this memory 1 is constituted from m words (from WO to W255) in which each WORD is formed of b basic memory cells by l lines which each line consisted of.
[0027] By the standard approach, b becomes an integer equal to the power of l, m, and2. Hereafter, it is referred to as l=m=24=16 and b=23=8 in explanation.
[0028] The address ADD typically encoded by k bits with which are satisfied of 2 k=l*m is given for every WORD. Please understand that it is referred to as k= 8, 4 bits of high orders of the address determine a line to choose, and 4 bits of low order of the address determine WORD to read in the line to choose in the following explanation.
[0029] According to this invention, this approach starts decode of that address ADD, when the first q (=k-p) bit of Address ADD is received. Here, q and p are integers and p<k. There is 2 k word in memory. There are 2 p words of WORD which has the address where these q address bit and the first q address bit which were received are the same to q address bit. Therefore, based on the received first q address bit, a 2p piece binary information element is taken out.
[0030] Therefore, WORD is divided into 2 p word group, and, as for each WORD group, a read-out circuit is prepared as follows. In each WORD group, the remaining p address bits of the WORD from which, as for WORD, the first q address bit differs mutually are the same. In the example, p is equal to 1.
[0031] Therefore, supposing it receives Address ADD serially, decode of this address will be started before the least significant bit appears in an input yet. In this condition, while this can determine certainly the line which should be chosen based on the received first bit, it means that the uncertainty of a certain extent remains about specific WORD to read. the case of p= 1 -- memory -- a two half (memory) -- an array -- it is formed of M1 and M2, and the half-array M1 corresponds to the room where the last address bit is equal to 1, and the half-array M2 of another side is considered to correspond to the room where the last address bit is equal to 0. A memory array is divided into an even parity half array and an odd parity half array.
[0032] Memory 1 is a standard approach about the binary information element DATA corresponding to the address ADD which received the address ADD of one WORD to read with the serial ****** address input terminal 2 and input register RI which receives an address bit. The data output terminal 3 outputted outside serially and the input terminal 4 which receives the clock signal CLK which occurs in the exterior of memory and sets up the working speed of memory 1, The input terminal 5 (in one example) which receives the read-out control-logic signal READ The line decoding circuit LD which chooses one of l lines of each ** array at the time of READ=1 as the WORD of memory is read, and two multiplexers (namely, 2p) MUX1 and MUX2 are controlled. The train decoding circuit CD which chooses 1 word which should read of the lines chosen by the line decoding circuit for every half-array by these multiplexers is provided.
[0033] The control circuit CC where memory 1 sends further the control signal which synchronizes actuation of memory 1 appropriately in response to a clock signal CLK and the read-out control signal READ to various circuits in memory In order to take two binary data components, to come out and to carry out from two selected WORD, Two read-out circuits SA1

and SA2 where one was attached to one of the half-arrays M1 and M2, respectively, One of the taken-out 2p binary information elements is chosen (following the condition of the selection signal received from the control circuit CC). It has the output multiplexer MUXS and output register RO which have 2p parallel input and one parallel output for outputting outside the information element taken out and chosen. Typically, this output register is a shift register of a parallel input / serial output. The input of an output register RO is connected to the output of the output multiplexer MUXS, and the output of an output register RO is connected to the output terminal 3. (if the information element is encoded by b= 8 bits) According to the above-mentioned conditions, naturally, this output register RO is formed of eight cels.

[0034] Since a rank exception is satisfactory and this contractor can manufacture a circuit based on explanation of the following actuation, the detailed explanation of the logical organization of a circuit is omitted.

[0035] Input register RI is formed with the following two registers. That is, it is formed with the 2nd subregister RI 2 which has the 1st subregister RI 1 which has the serial input which stores the first q bits of the received address ADD, and a parallel output, the serial input which stores the remaining [k-q] bits of the received address ADD, and a parallel output (formed only of one cel).

[0036] Two subregisters RI1 and RI2 are shift registers which connected the input to the address input terminal 2, respectively.

[0037] The parallel output of the subregister RI 1 is connected to the decoding circuits LD and CD. Four of the cels of the subregister RI 1 are connected to the line decoding circuit LD, and other three cels are connected to the train decoding circuit CD. In addition, in order that a train decoding circuit may process not 4 bits but a triplet as compared with the standard memory which has an equivalent capacity, please note that size is small.

[0038] The subregister RI 1 receives the shift control-logic signal SR 1. At the time of SR 1= 1, the contents of the cel answer the first transition of a clock signal, and are shifted at a time one cel.

[0039] The parallel output (in the case of this example, since it is k-q=1, it is a serial output) of the subregister RI 2 is connected to a control circuit CC. AD0 is the contents of the subregister RI 2. The subregister RI 2 receives the shift control-logic signal SR 2. At the time of SR 2= 1, the contents of the cel answer the first transition of a clock signal, and are shifted at a time one cel.

[0040] These bits are stored in the subregister RI 1 when the first q address bit of memory without sequential read-out mode is received (when shown in drawing 1).

[0041] These bits are stored in the subregister RI 2 when the remaining p address bits are received. At this time, a control signal SR 1 is held at a condition equal to 0, and the contents of the subregister RI 1 are made not to be changed.

[0042] Read-out of WORD consists of the next phase.

** Serially in response to the fact that the first 7 address bit of WORD to read, store in the 1st subregister RI 1 (SR 1= 1).

** Are concurrent with what (SR 2= 1 and SR 1= 0) is stored in the cel of the 2nd subregister RI 2 in response to the last address bit. The first 7 address bit of a carrier beam is decoded by the line decoding circuit LD and the train decoding circuit CD. Swerve from the read-out circuits SA1 and SA2 to the WORD of the two half-arrays M1 and M2 whose first seven addresses correspond with the first 7 address bit of a carrier beam, and it it-connects. The binary information element expressed by these two WORD is taken out by the read-out circuits SA1

and SA2. ** Decode the remaining address bits (AD0) by the control circuit CC (). That is, the selection signal given to an output multiplexer is generated and the binary information element expressed according to the contents of the WORD which has the address which is in agreement with received 8 address bit is outputted to the output-data terminal 3 by the output multiplexer MUXS and the output register RO. In fact, since it is p= 1, the output multiplexer MUXS can be controlled directly by connecting the output of the subregister RI 2 to the control input of the output multiplexer MUXS.

[0043] The example shown in drawing 1 is explained as one example. In fact, most commercial serial access memory operates in sequential read-out mode.

[0044] There are the following differences as compared with memory drawing 1 with sequential read-out mode (when shown in drawing 2). Memory has the control input terminal 6 which receives the control-logic signal SR which can go into sequential read-out mode. SR=1 shall correspond to sequential read-out mode. Input register RI operates as a binary address counter. The 1st and 2nd subregister RI1 and RI2 is not a mere shift register. It assumes that the contents of the subregisters RI1 and RI2 can change sequential read-out mode inside memory. Input register RI is controlled by the control circuit CC, and it will make an automatic (being increment 1 typically) change of the contents of said counter (if Signal INC is a logic state 1). (control-logic signal INC)

[0045] The subregisters RI1 and RI2 increment one unit of the (answering the first transition of for example, a control-logic signal) contents in response to the control-logic signal INC.

[0046] The subregister RI 2 has one output which outputs the digit riser logic signal CRI2 further again. All the bits in which this signal CRI2 was stored in this register after the increment of the contents of the subregister RI 2 will be in the predetermined condition 1, for example, a condition, when it is zero (0). Before an increment, this corresponds, when all the bits stored in this register are 1. Generally, this is equivalent to changing the contents of the subregister RI 1 to read the WORD in the next address of the address of the WORD read before the increment. Therefore, in addition to Signal INC, a signal CRI2 is given to the subregister RI 1, the first transition of INC and CRI 2= 1 is answered only at the time of INC and CRI 2= 1, and the increment of the contents of the subregister RI 1 is carried out to coincidence. The read-out circuits SA1 and SA2 receive respectively the read-out control signal expressed with READ1 and READ2, respectively.

[0047] It is performed as follows. : READ1=SR*READ*AD0+READ*/SR READ2=SR*READ*/AD0+READ*/SR* expresses an AND, + expresses an OR, and / expresses a reversal signal.

[0048] The address can divide into two cases about the ejection of the information from the address by whether it is given to memory with the address input terminal 2, or it generates inside.

[0049] 1 When receiving the address from the exterior, this example is equivalent to the same mode of operation as the actuation shown in drawing 1 .

[0050] By the approach same in order to read WORD as the example shown in drawing 1 , q bits of the start are used by line decoding and the train decoding circuits LD and CD, and the remaining p bits are used by the control circuit CC.

[0051] When the information element of 2p taken out from the memory cell is read (it is READ1=READ2=READ, of course), the information corresponding to received k bits is stored in an output register RO by the output multi-pre sir MUXS (selection by ADD). Subsequently, an information element is outputted to a data output terminal by the shift in an output register RO.

[0052] 2 the output of the information element corresponding to the address first given in sequential read-out sequential read-out mode -- then, the address is changed without the mediation from the outside so that other information elements may be outputted outside continuously.
[0053] Like before, the first above-mentioned address presupposes that 1 unit increment is carried out in order to give the information stored in the WORD in the next address.
[0054] The next phase is performed.
** Output the information which corresponds in response to k address bit from the exterior to a data output terminal.
** Increment the one unit of the contents of the 2nd subregister RI 2 in parallel to the output of the information on a data output terminal. The 1st subregister RI 1 is incremented conditionally (as the function of CRI2). after an increment and the contents of the subregister RI 1 -- decoding -- ** -- request information is taken out by the read-out circuits SA1 or SA2 suitable as a function of the contents AD 0 of the subregister RI 2 after an increment which determine the condition of READ1 and READ2.
[0055] For example, an increment can be carried out if the one half of the information bit memorized by the output register is actually outputted to the data output terminal. An important thing is not waiting for the output of the last bit of an output register, and not performing the next read-out actuation. this lowers a maximum-permissible clock frequency effectively -- things -- ** In other words, also in sequential read-out mode, there is an advantage from which the profits of the internal access time equal to the internal access time in the case of un-sequential read-out mode (from the outside to the ********** case [The address / Or correctly]) at least are obtained.
[0056] In the illustrated example, the carrier beam assumption of the 1st address (AD0 passing zero) of the 1st WORD of a half-array is carried out from the outside. The increment (AD0 passing one) of this 1st address gives the 2nd address of the 2nd WORD in the half-array M1. The first q bits of the 1st and 2nd address are the same. In order to read the contents of the 2nd WORD, q bits stored in the subregister RI 1 are not changed (CRI 2= 0). It is READ1=/READ 2= 1.
[0057] The following phase is performed in order to read the following WORD in the half-array M2.
** Increment the contents of the subregister RI 2 (AD [0= 0] and CRI 2= 1) with a control signal INC, and it is the subregister RI 1 (with the q-th address bit). Probably the contents of modification of one or more bits in other address bits are incremented. q bits stored in the subregister RI 1 after an increment are decoded by the decoding circuits LD and CD. ** By the ** read-out circuit SA 2 (READ2=/READ 1= 1) The binary information which took out the WORD corresponding to the address after an increment to read-out and a ** output register is stored, and ** information is outputted.
[0058] Of course, this invention is not limited to the above-mentioned example, and it can be performed, without deviating from the design for this invention from other amelioration and escapes. Especially a memory cell can be constituted in the group of three or more a large number. In this case, the access time seen inside memory increases, power consumption also corresponded and the occupancy tooth space of memory also increases.
[0059] It is possible to use 2p output register, to attach one of the read-out circuits to the each further again, and to prepare an output multiplexer between these output registers and a data output terminal. 2p word can always be then outputted to read-out and a data output terminal in

sequential read-out mode at continuation of these WORD. Therefore, unless the first q address bit is changed, effective read-out is not made.

TECHNICAL FIELD

[Field of the Invention] This invention relates to serial access memory. Although especially this invention can be adapted for memory volatile [of other formats], or non-volatile, it relates to eliminable programmable read-only memory (EEPROMs) electrically.

PRIOR ART

[Description of the Prior Art] (from a number of an information element of standpoints memorized) Current development of the memory of the integrated-circuit format of having a very large information storage capacity is furthered by the request which wants to make high the frequency of the clock signal which determines the working speed of the system incorporating these integrated-circuits memory. Consequently, coincidence also has the research which shortens increasingly time amount which accesses the contents of the WORD which constitutes these memory. "WORD" means a physical stereo with the contents showing the binary information element encoded by b bits here. b is an integer here. WORD is formed of b basic memory cells, and each basic memory cell is typically formed of a store circuit.
[0003] Seeing from the access time, parallel access memory is the most advantageous memory. The period corresponding to 1 cycle of the clock signal which determines the working speed of such memory is enough to give one of the memory of these for the one address which is the WORD from which the contents are read in parallel.
[0004] Nevertheless, as for serial access memory, that a manufacture price is low, that a package is especially small light clearly, etc. have a clear advantage again as compared with parallel access memory. In fact, there are very few contact pins which need serial memory. The number of contact pins of an integrated circuit affects extremely the amount of space which an integrated circuit occupies. Consequently, serial access memory is very useful portable.
[0005] However, it is desirable that the clock signal frequency and storage capacity of these serial access memory can be increased. Memory capacity is 64 kilobits and the present most highly efficient product operates on the frequency of about 1MHz. The frequency more than the storage capacity and the 5MHz range of about 256 kilobits is expectable in the near future.
[0006] In fact, the technical issue essentially involved to the access time to the contents of WORD in read-out mode produces increase of the clock signal frequency of these memory. The time of the address of WORD being known by memory with the "access time" in "read-out mode" (at namely, the time of memory receiving all the address bits of WORD serially), Please understand that the period seen in the exterior between the time of the binary information which the contents of the memory cell of WORD express beginning to become available (when memory being serial output memory), or the time of becoming available in the exterior of memory through one or more output pins (when memory being parallel output memory or the information element being encoded by 1 bit) is meant.
[0007] The access time is essentially restricted by time amount required to perform the following

two phases in order.
- Switch appropriately various change equipments for connecting a read-out circuit to the WORD which has decoding the address which memory received, i.e., the contents showing binary information reading.
- The binary information on a logic signal format is taken out from an original read-out process, i.e., the read WORD, (the memory cell of WORD does not necessarily memorize a directly usable logic information element, but, generally the metaphor has the physical characteristic which is changed into a logic signal by the suitable circuit which consists of differential amplifier and which can be changed).

[0008] By the standard approach, the address encoded by the bit of a certain number can receive serially with a shift register. Only many clock signal cycles of the number as the address bit which can be received with this same approach continue.

[0009] The maximum-permissible access time is often equal to an odd times as many duration as the half cycle of a clock signal. For example, this access time is set as 3 half cycles, when memory is connected to the micro wire or the I2C mold bus, and when memory is connected to the SPI bus, it is set as a half cycle.

[0010] Therefore, the format of a bus that memory communicates with other equipments determines the maximum-permissible access time to a given clock signal frequency. For example, the permission access time is restricted to 250 nanoseconds and this corresponds to the engine-performance level near the engine-performance level of the equipment which reads high-speed parallel access memory to use an SPI bus and the clock signal frequency of 2MHz.

[0011] Technical difficulty arises in structure peculiar to a required toggling speed. If there is a solution means, the circuit used is a high power consumption circuit in many cases. In the memory often constituted by portable [which is asked for the minimum power consumption level], this is hardly desirable. The frequency of a clock signal is determined to the maximum-permissible access time it is expected in fact therefore that is the format of the bus used.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The purpose of this invention is offering the standard configuration of the conventional serial access memory, the standard read-out approach, the same configuration of serial access memory as a functional target, and the read-out approach, when the above-mentioned technical issue is solved, and it has technical conciseness and low power consumption and they are seen from the outside.

MEANS

[Means for Solving the Problem] Each memory is constituted by two or more words at the form of a matrix, and the contents of each WORD express a binary information element. Each WORD can access in the address encoded by k bits in binary mode (k is a larger integer than 1). The approach by this invention which reads the contents of the WORD of integrated-circuit memory that an address bit is serially supplied to memory through an address input terminal Are concurrent with receiving serially the first q bits of the 1-word address to read (q being an integer

smaller than k), and receiving the remaining [k-q] bits of said address, in order to read the 1-word contents. Decode the first [said] q bits of said received address, and a read-out circuit is connected to the WORD which has the first q address bit corresponding to the first [said] q bits of said received address. Take out the binary information element which the contents of said WORD express, and while decoding said remaining [k-q] bits of said 1 word [to read] address Said binary information element which said contents of said WORD which has an address bit corresponding to the first [said] q bits of said received address express is outputted to the data output terminal of memory.

[0014] Therefore, before the address bit has received this invention altogether yet, it proposes starting address decode and read-out. Therefore, internal enhancement is attained from the standpoint of the number of half cycles of a clock signal in the interior access time of the maximum permissible (namely, the maximum time amount of read-out of address decode and WORD), and the maximum-permissible access time is still the same to a given frequency seen from the exterior of memory. Therefore, the access time seen from the outside is not determined any longer depending on the activation period of address decode and read-out actuation, but is smaller than the activation period. therefore -- being the same in the maximum access time by this -- carrying out -- a case -- a permissible clock signal frequency -- it can increase . Since it starts to coincidence before the address bit has received all for decode yet, in order to take out information from all the WORD that have an address bit corresponding to the received bit, to it, some read-out circuits stand in a row and operate at the time of initiation of decode. The information outputted from an output is chosen when the whole address is found. Then, easy short-time re-routing is performed as compared with original decode and actuation of read-out, and the access time is mainly restricted by the lateness of the same actuation as use of a sense amplifier etc.

[0015] Furthermore, according to this invention, it is constituted by two or more words and the contents of each WORD express a binary information element. The address input terminal which each WORD can access in the address encoded by k bits in binary mode (k is a larger integer than 1) and which is integrated-circuit memory and receives an address bit serially, The data output terminal which outputs the binary information element corresponding to the contents of the WORD by which the address was carried out, In the integrated-circuit memory possessing the input register which memorizes a carrier beam address bit, the circuit which decodes the received address bit, and the circuit linked to the circuit which reads WORD Said WORD is constituted by two or more WORD groups, and the first k address bits of the WORD contained in each WORD group differ mutually. If the remaining [k-q] address bits are the same (q is an integer smaller than k), a read-out circuit is prepared for every WORD group and memory receives k address bit Said read-out circuit takes out the binary information expressed according to the contents of the WORD group corresponding to the first k address bit of a carrier beam. The control-output multiplexing circuit where memory outputs the binary information expressed according to the contents of the WORD which has the address corresponding to received k bits further to said data output terminal is provided.

[0016] The above-mentioned memory enforces the above-mentioned approach. Since some read-out circuits where the memory according to this invention as compared with standard memory operates to juxtaposition exist, a dimension becomes large slightly. however -- it should observe -- actuation is the technical simplicity of the same memory of this as actuation of memory standard as a whole. In order to make a permissible clock signal frequency high, the read-out circuit of the same format as standard memory can be used. This means that increase of power

consumption is not what depends only on the number of the read-out circuits used increasing, and is depended on what the complexity of the circuit of memory increased.
[0017] q-bit decode of the start of the addresses of WORD to read can actually be carried out in a standard line decoding circuit and a train decoding circuit. Decode of the [k-q] bit of the carrier beam remainder corresponds to generating of the control signal for a multiplexing circuit and a read-out circuit.
[0018] The received address bit is memorized in standard memory by the shift register formed from k cels. This shift register is connected to an address input terminal. For the memory which can operate in sequential read-out mode, further, this input register is constituted so that it can operate as a binary address counter.
[0019] In a desirable mode, this invention memorizes [1st] the remaining [k-q] address bits to the 2nd of the first q address bit. Therefore, two shift subregisters which have q cel and the [k-q] cel, respectively are used. Two subregisters are connected to an address input terminal. By this configuration, it becomes memorizable [the address bit of the same line as the always same cel]. Thereby, this invention can carry out easily. In fact, it becomes still more complicated to use a single shift register so that the first q address bit may be supplied shortly after the q-th bit won popularity. When using a single shift register, the contents of the cel of this register will be changed by shift, decoding. In order to secure the stability of q bits used for decode in fact therefore, it is required to prepare a buffer register between an input register and a decoder circuit.
[0020] It has q cel and actuation cannot be limited to the input register of the single shift register mold by which direct continuation was carried out to the address input terminal further again. In order to secure the stability of the bit used [1st] for decode of the address, it is required for the received first q address bit to be memorizable. In order to enable it to control an output multiplexing circuit to the 2nd by the clear (k-q> if it to be 1) and stable approach, it is required for it for the received remaining [k-q] address to be also memorizable.
[0021] In a desirable mode, this invention offers how memory has the so-called sequential read-out mode in which memory outputs automatically the 2nd binary information element expressed according to the contents of the 2nd WORD of memory to a data output terminal after read-out of the contents of the 1st WORD corresponding to the 1st address.
[0022] The stored address is changed automatically and serial access memory has without external mediation read-out mode with which the information element corresponding to the contents of the WORD which continues after that is outputted automatically, shortly after the address received from the exterior is stored in an address counter and the information corresponding to the received address is outputted outside. Modification of the address actually has the most common increment of the address.
[0023] This invention provides coincidence with the memory whose input registers are ** and a binary address counter.
[0024] Of course, unlike the case of standard memory, there is no modification on the approach of the contents of the q cel of the subregister corresponding to the first q address bit with sequential read-out mode. These contents are not changed unless it has the first q address bit in which the 2nd WORD differs from the 1st WORD. The stored remaining [k-q] bits are used in order that modification of the first q address bit may distinguish whether it is the need.
[0025]
[Embodiment of the Invention] Drawing 1 and drawing 2 show the memory 1 which is the EEPROM mold memory manufactured by well-known semiconductor technology.

[0026] For example, this memory 1 is constituted from m words (from WO to W255) in which each WORD is formed of b basic memory cells by l lines which each line consisted of.
[0027] By the standard approach, b becomes an integer equal to the power of l, m, and2. Hereafter, it is referred to as l=m=24=16 and b=23=8 in explanation.
[0028] The address ADD typically encoded by k bits with which are satisfied of 2 k=l*m is given for every WORD. Please understand that it is referred to as k= 8, 4 bits of high orders of the address determine a line to choose, and 4 bits of low order of the address determine WORD to read in the line to choose in the following explanation.
[0029] According to this invention, this approach starts decode of that address ADD, when the first q (=k-p) bit of Address ADD is received. Here, q and p are integers and p<k. There is 2 k word in memory. There are 2 p words of WORD which has the address where these q address bit and the first q address bit which were received are the same to q address bit. Therefore, based on the received first q address bit, a 2p piece binary information element is taken out.
[0030] Therefore, WORD is divided into 2 p word group, and, as for each WORD group, a read-out circuit is prepared as follows. In each WORD group, the remaining p address bits of the WORD from which, as for WORD, the first q address bit differs mutually are the same. In the example, p is equal to 1.
[0031] Therefore, supposing it receives Address ADD serially, decode of this address will be started before the least significant bit appears in an input yet. In this condition, while this can determine certainly the line which should be chosen based on the received first bit, it means that the uncertainty of a certain extent remains about specific WORD to read. the case of p= 1 -- memory -- a two half (memory) -- an array -- it is formed of M1 and M2, and the half-array M1 corresponds to the room where the last address bit is equal to 1, and the half-array M2 of another side is considered to correspond to the room where the last address bit is equal to 0. A memory array is divided into an even parity half array and an odd parity half array.
[0032] Memory 1 is a standard approach about the binary information element DATA corresponding to the address ADD which received the address ADD of one WORD to read with the serial ****** address input terminal 2 and input register RI which receives an address bit. The data output terminal 3 outputted outside serially and the input terminal 4 which receives the clock signal CLK which occurs in the exterior of memory and sets up the working speed of memory 1, The input terminal 5 (in one example) which receives the read-out control-logic signal READ The line decoding circuit LD which chooses one of l lines of each ** array at the time of READ=1 as the WORD of memory is read, and two multiplexers (namely, 2p) MUX1 and MUX2 are controlled. The train decoding circuit CD which chooses 1 word which should read of the lines chosen by the line decoding circuit for every half-array by these multiplexers is provided.
[0033] The control circuit CC where memory 1 sends further the control signal which synchronizes actuation of memory 1 appropriately in response to a clock signal CLK and the read-out control signal READ to various circuits in memory In order to take two binary data components, to come out and to carry out from two selected WORD, Two read-out circuits SA1 and SA2 where one was attached to one of the half-arrays M1 and M2, respectively, One of the taken-out 2p binary information elements is chosen (following the condition of the selection signal received from the control circuit CC). It has the output multiplexer MUXS and output register RO which have 2p parallel input and one parallel output for outputting outside the information element taken out and chosen. Typically, this output register is a shift register of a parallel input / serial output. The input of an output register RO is connected to the output of the

output multiplexer MUXS, and the output of an output register RO is connected to the output terminal 3. (if the information element is encoded by b= 8 bits) According to the above-mentioned conditions, naturally, this output register RO is formed of eight cels.
[0034] Since a rank exception is satisfactory and this contractor can manufacture a circuit based on explanation of the following actuation, the detailed explanation of the logical organization of a circuit is omitted.
[0035] Input register RI is formed with the following two registers. That is, it is formed with the 2nd subregister RI 2 which has the 1st subregister RI 1 which has the serial input which stores the first q bits of the received address ADD, and a parallel output, the serial input which stores the remaining [k-q] bits of the received address ADD, and a parallel output (formed only of one cel).
[0036] Two subregisters RI1 and RI2 are shift registers which connected the input to the address input terminal 2, respectively.
[0037] The parallel output of the subregister RI 1 is connected to the decoding circuits LD and CD. Four of the cels of the subregister RI 1 are connected to the line decoding circuit LD, and other three cels are connected to the train decoding circuit CD. In addition, in order that a train decoding circuit may process not 4 bits but a triplet as compared with the standard memory which has an equivalent capacity, please note that size is small.
[0038] The subregister RI 1 receives the shift control-logic signal SR 1. At the time of SR 1= 1, the contents of the cel answer the first transition of a clock signal, and are shifted at a time one cel.
[0039] The parallel output (in the case of this example, since it is k-q=1, it is a serial output) of the subregister RI 2 is connected to a control circuit CC. AD0 is the contents of the subregister RI 2. The subregister RI 2 receives the shift control-logic signal SR 2. At the time of SR 2= 1, the contents of the cel answer the first transition of a clock signal, and are shifted at a time one cel.
[0040] These bits are stored in the subregister RI 1 when the first q address bit of memory without sequential read-out mode is received (when shown in drawing 1).
[0041] These bits are stored in the subregister RI 2 when the remaining p address bits are received. At this time, a control signal SR 1 is held at a condition equal to 0, and the contents of the subregister RI 1 are made not to be changed.
[0042] Read-out of WORD consists of the next phase.
** Serially in response to the fact that the first 7 address bit of WORD to read, store in the 1st subregister RI 1 (SR 1= 1).
** Are concurrent with what (SR 2= 1 and SR 1= 0) is stored in the cel of the 2nd subregister RI 2 in response to the last address bit. The first 7 address bit of a carrier beam is decoded by the line decoding circuit LD and the train decoding circuit CD. Swerve from the read-out circuits SA1 and SA2 to the WORD of the two half-arrays M1 and M2 whose first seven addresses correspond with the first 7 address bit of a carrier beam, and it it-connects. The binary information element expressed by these two WORD is taken out by the read-out circuits SA1 and SA2. ** Decode the remaining address bits (AD0) by the control circuit CC (). That is, the selection signal given to an output multiplexer is generated and the binary information element expressed according to the contents of the WORD which has the address which is in agreement with received 8 address bit is outputted to the output-data terminal 3 by the output multiplexer MUXS and the output register RO. In fact, since it is p= 1, the output multiplexer MUXS can be controlled directly by connecting the output of the subregister RI 2 to the control input of the

output multiplexer MUXS.
[0043] The example shown in drawing 1 is explained as one example. In fact, most commercial serial access memory operates in sequential read-out mode.
[0044] There are the following differences as compared with memory drawing 1 with sequential read-out mode (when shown in drawing 2). Memory has the control input terminal 6 which receives the control-logic signal SR which can go into sequential read-out mode. SR=1 shall correspond to sequential read-out mode. Input register RI operates as a binary address counter. The 1st and 2nd subregister RI1 and RI2 is not a mere shift register. It assumes that the contents of the subregisters RI1 and RI2 can change sequential read-out mode inside memory. Input register RI is controlled by the control circuit CC, and it will make an automatic (being increment 1 typically) change of the contents of said counter (if Signal INC is a logic state 1). (control-logic signal INC)
[0045] The subregisters RI1 and RI2 increment one unit of the (answering the first transition of for example, a control-logic signal) contents in response to the control-logic signal INC.
[0046] The subregister RI 2 has one output which outputs the digit riser logic signal CRI2 further again. All the bits in which this signal CRI2 was stored in this register after the increment of the contents of the subregister RI 2 will be in the predetermined condition 1, for example, a condition, when it is zero (0). Before an increment, this corresponds, when all the bits stored in this register are 1. Generally, this is equivalent to changing the contents of the subregister RI 1 to read the WORD in the next address of the address of the WORD read before the increment. Therefore, in addition to Signal INC, a signal CRI2 is given to the subregister RI 1, the first transition of INC and CRI 2= 1 is answered only at the time of INC and CRI 2= 1, and the increment of the contents of the subregister RI 1 is carried out to coincidence. The read-out circuits SA1 and SA2 receive respectively the read-out control signal expressed with READ1 and READ2, respectively.
[0047] It is performed as follows. : READ1=SR*READ*AD0+READ*/SR READ2=SR*READ*/AD0+READ*/SR* expresses an AND, + expresses an OR, and / expresses a reversal signal.
[0048] The address can divide into two cases about the ejection of the information from the address by whether it is given to memory with the address input terminal 2, or it generates inside.
[0049] 1 When receiving the address from the exterior, this example is equivalent to the same mode of operation as the actuation shown in drawing 1 .
[0050] By the approach same in order to read WORD as the example shown in drawing 1 , q bits of the start are used by line decoding and the train decoding circuits LD and CD, and the remaining p bits are used by the control circuit CC.
[0051] When the information element of 2p taken out from the memory cell is read (it is READ1=READ2=READ, of course), the information corresponding to received k bits is stored in an output register RO by the output multi-pre sir MUXS (selection by ADD). Subsequently, an information element is outputted to a data output terminal by the shift in an output register RO.
[0052] 2 the output of the information element corresponding to the address first given in sequential read-out sequential read-out mode -- then, the address is changed without the mediation from the outside so that other information elements may be outputted outside continuously.
[0053] Like before, the first above-mentioned address presupposes that 1 unit increment is carried out in order to give the information stored in the WORD in the next address.

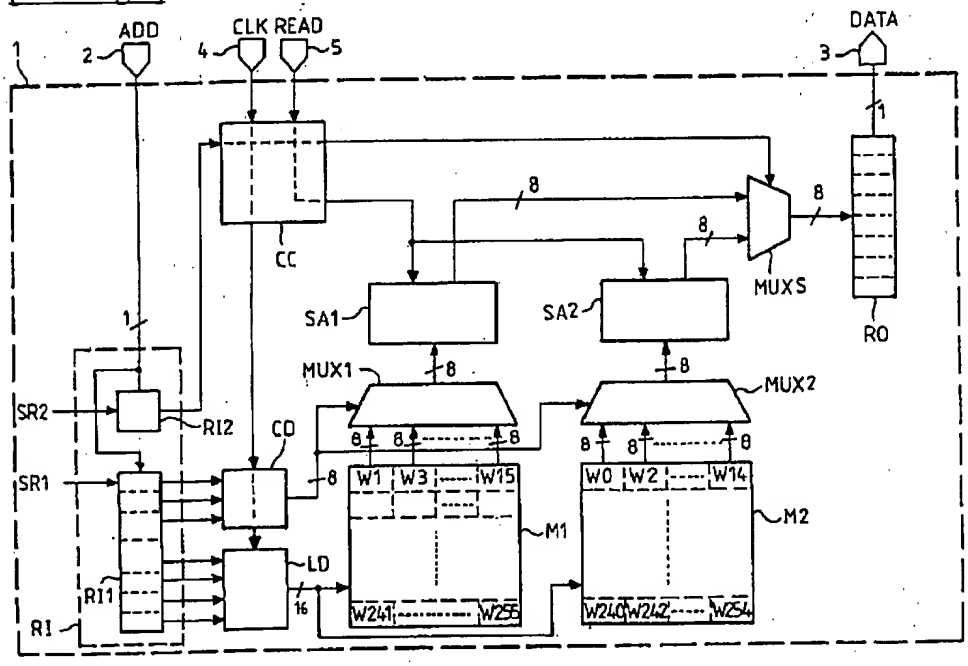
[0054] The next phase is performed.
** Output the information which corresponds in response to k address bit from the exterior to a data output terminal.
** Increment the one unit of the contents of the 2nd subregister RI 2 in parallel to the output of the information on a data output terminal. The 1st subregister RI 1 is incremented conditionally (as the function of CRI2). after an increment and the contents of the subregister RI 1 -- decoding -- ** -- request information is taken out by the read-out circuits SA1 or SA2 suitable as a function of the contents AD 0 of the subregister RI 2 after an increment which determine the condition of READ1 and READ2.
[0055] For example, an increment can be carried out if the one half of the information bit memorized by the output register is actually outputted to the data output terminal. An important thing is not waiting for the output of the last bit of an output register, and not performing the next read-out actuation. this lowers a maximum-permissible clock frequency effectively -- things -- ** In other words, also in sequential read-out mode, there is an advantage from which the profits of the internal access time equal to the internal access time in the case of un-sequential read-out mode (from the outside to the ********** case [The address / Or correctly]) at least are obtained.
[0056] In the illustrated example, the carrier beam assumption of the 1st address (AD0 passing zero) of the 1st WORD of a half-array is carried out from the outside. The increment (AD0 passing one) of this 1st address gives the 2nd address of the 2nd WORD in the half-array M1. The first q bits of the 1st and 2nd address are the same. In order to read the contents of the 2nd WORD, q bits stored in the subregister RI 1 are not changed (CRI 2= 0). It is READ1=/READ 2= 1.
[0057] The following phase is performed in order to read the following WORD in the half-array M2.
** Increment the contents of the subregister RI 2 (AD [0= 0] and CRI 2= 1) with a control signal INC, and it is the subregister RI 1 (with the q-th address bit). Probably the contents of modification of one or more bits in other address bits are incremented. q bits stored in the subregister RI 1 after an increment are decoded by the decoding circuits LD and CD. ** By the ** read-out circuit SA 2 (READ2=/READ 1= 1) The binary information which took out the WORD corresponding to the address after an increment to read-out and a ** output register is stored, and ** information is outputted.
[0058] Of course, this invention is not limited to the above-mentioned example, and it can be performed, without deviating from the design for this invention from other amelioration and escapes. Especially a memory cell can be constituted in the group of three or more a large number. In this case, the access time seen inside memory increases, power consumption also corresponded and the occupancy tooth space of memory also increases.
[0059] It is possible to use 2p output register, to attach one of the read-out circuits to the each further again, and to prepare an output multiplexer between these output registers and a data output terminal. 2p word can always be then outputted to read-out and a data output terminal in sequential read-out mode at continuation of these WORD. Therefore, unless the first q address bit is changed, effective read-out is not made.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The memory configuration by this invention is shown.
[Drawing 2] Other memory configurations by this invention which can use sequential read-out mode are shown.
[Description of Notations]
1 Memory
2 Address Input Terminal
3 Data Output Terminal
4 Five Input terminal
6 Control Input Terminal
RI Input register
LD Line decoding circuit
CD Train decoding circuit
SA Read-out circuit
MUXS Output multiplexer
RO Output register

DRAWINGS

[Drawing 1]



[Drawing 2]